CMOS Preamplifier for Low-Capacitance Detectors*

G. Gramegna[1], P. O'Connor[2], P. Rehak[2], S. Hart[3]

[1] Politecnico. di Bari, Italy [2] BNL, USA [3] Wayne State Univ., USA

ABSTRACT

We present a new CMOS preamplifier and shaper, optimized for charge measurements with detectors of 0.1-1 pF capacitance. A self-adaptive biasing scheme with nonlinear pole-zero cancellation allows us to use an MOS device operated in the triode region as the DC feedback element while eliminating nonlinearity and sensitivity to supply, temperature, and process variations and accepting up to several μA leakage current. The circuit is continuously sensitive and requires no external adjustments to set the feedback resistance. Secondary sources of noise are minimized subject to a power dissipation constraint.

Implemented in a 1.2 μm CMOS process, the preamplifier achieves an ENC of 35 e^- + 58 e^-/pF at 23 μs shaping time at a power consumption of about 3.2 mW. The integrated preamp/shaper has 50 ns shaping time and the ENC is 120 e^-. It has 0.3% nonlinearity over an input dynamic range of 0 - 50 fC.

I. Introduction

Low-capacitance silicon detectors are finding applications for particle position sensing, X-ray spectroscopy, and X-ray imaging. In particular, silicon drift detectors (SDD) [1] offer a remarkable combination of large sensitive area with extremely small anode size, leading to capacitances on the order of 0.1 pF. To take full advantage of the low capacitance of these devices, the readout electronics must meet several criteria:

---

* This work supported by U.S. DOE Contract No. DE-AC02-67CH00016

1. Can be directly wirebonded to the detector anodes.
2. Input transistor is properly capacitance-matched to the detector.
3. Able to accept the detector leakage current without generating excess parallel noise.

If condition (1) or (2) is not met, the series noise will be excessive. Failure to meet condition (3) means the parallel noise will be dominated by the feedback resistance of the amplifier rather than the detector leakage current.

For fabricating this type of readout circuit, CMOS technology offers the advantages of being inexpensive and readily available for full custom designs. The input transistor dimensions, and the physical arrangement of the circuit and bond pads, can be optimized to meet criteria (1) and (2) above. However, there are several compensating disadvantages of CMOS for low-noise charge-sensitive preamplifiers. First, its 1/f noise is high in comparison to other technologies. Second, it dissipates more power to achieve the same noise. Finally, as in all IC technologies there is no simple way to create the high-value feedback resistor that is required to satisfy condition (3) above.

The CMOS circuit that we describe here addresses these problems, in particular by using novel circuit techniques to create a stable, linear feedback resistance.

Although this circuit was developed as a general-purpose amplifier for low-capacitance detectors with fast shaping, the design of the prototype was geared towards the requirements of a vertex tracking detector in a heavy-ion collider experiment [2]. This experiment will use multi-anode SDDs to reconstruct particle tracks with a position resolution of less than 25 μm. The requirements are shown in Table 1.

II. Circuit Design

II.1 Preamplifier

II.1.1 Folded Cascode Stage

This stage (Fig. 1) is a charge-sensitive preamplifier based on a single-ended folded cascode. We expected the noise to be dominated by the series thermal noise of the input transistor, so we chose an NMOS device which provides higher transconductance than the complementary PMOS at the same drain current. To optimize the noise for a constant drain current, we selected the input transistor's width to give a gate capacitance about 1/3 of that of the detector plus parasitics [3]. This device is biased at a drain current of about 0.4 mA to give a transconductance of 3.5 mS.

The most important secondary noise sources in the preamp are the current sources M4 and M6, whose noise contribution can be minimized by source degeneration. We used an analytic procedure to design these degenerated current sources for lowest possible noise under the constraint of constant power dissipation.

The open-loop voltage gain of the preamplifier is

$$A_v(s) = \frac{g_{m1}R_0}{(1+s\tau_1)(1+s\tau_2)} \bullet \frac{R_{o1}}{(R_{o1}+R_{icas})} \tag{1}$$

and the two poles are given by:

$$\tau_1 = R_0 C_0, \tag{2}$$

$$\tau_2 = R_{icas} C_1$$

where g_{m1} is the transconductance of M1. R_{o1} is the output resistance of M1 in parallel with the output resistance of M4, R_0 and C_0 are the effective resistance and capacitance seen from node DM6 to ground, and C_1 is the effective capacitance at node DM1. R_{icas}, the input resistance of the cascode transistor MCAS, is inversely proportional to g_{mcas}. This stage has a

gain of about 700, a gain-bandwidth product of 275 MHz, and dissipates about 3.1 mW. The feedback capacitor C_F is 0.1 pF. With an input capacitance of 0.8 pF representing the detector plus parasitics, the rise time to a charge impulse is 12 nsec.

II.1.2 Feedback Resistance

Choice of the feedback resistance is a tradeoff between low parallel noise (large R) and low DC voltage drop due to leakage current (smaller R):

$$\Delta V_{DC} = R \cdot I_L \tag{3}$$

$$4kT/R < 2qI_L \tag{4}$$

With leakage current I_L = 0 - 200 nA and ΔV_{dc} < 2V, this sets R in the range

$$250\ k\Omega < R < 10\ M\Omega \tag{5}$$

R does not have to be precisely defined, but it must stay in this range over worst-case process variations. Higher values of R are favored from the standpoint of noise.

In all monolithic technologies it is difficult to integrate a high-value resistor, so charge amplifiers need to use either a reset switch or a circuit block that behaves like a large resistance. Such a block can be a transconductor or a MOSFET operating in the so-called linear, triode, or non-saturated region ($V_{DS} < V_{GS} - V_T$). We concentrate on the non-saturated MOS resistor. In the absence of leakage current, its resistance is given by:

$$R = \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_T)} \tag{6}$$

where μ is the inversion layer mobility, C_{ox} is the gate capacitance per unit area, (W/L) is the FET width/length ratio, and (V_{GS}-V_T) is the gate bias voltage at equilibrium. Its sensitivity to control voltage fluctuations is:

$$\left|\frac{dR}{R}\right| = \mu C_{ox}\left(W/L\right)R \cdot \left|dV_{TOT}\right| \tag{7}$$

Here $dV_{TOT} = (dV_G + dV_S + dV_T)$ represents the total variation in the control voltage of the MOS resistor. In conventional triode-mode feedback schemes [4] V_G is derived from a supply voltage, which can have ±2% variation even in well-regulated systems. The other two terms in dV_{TOT} are set by MOSFET threshold voltages, which can vary about 150 mV from run to run. Using values of hole mobility μ_p = 200 cm^2/V-sec and gate capacitance C_{ox} = 1.7 fF/μm^2, and assuming that the overall supply and threshold variation totals 250 mV, we find

$$| dR/R | \sim 43\ (W/L) \tag{8}$$

for a target value of R = 5 MΩ. To keep R reasonably stable, say to ±20%, we must make W/L < 0.005. This extreme aspect ratio leads to a device whose active area is at least 200 W_{min}^2. In this technology such a device would have a gate capacitance of 200 $C_{ox}W_{min}^2$ = 1.1 pF. Since such a high capacitance would severely degrade the noise and gain linearity, it is not acceptable. To solve this we developed an adaptive gate bias circuit to stabilize the resistance against threshold and power supply variations. The circuit is illustrated in Fig. 2.

The goal of the bias circuit is to keep

$$V_{G2} - V_{S2} - V_{T2} = \text{const.} \tag{9}$$

even when V_{GS2}-V_{T2} is only a few times *kT/q*, as is necessary for large R with moderate W/L. Note that V_{S2} is determined mainly by the threshold of NMOS device M1, whose fluctuations are uncorrelated with V_{T2} of PMOS M2. The third term in (9), V_{T2}, is influenced by the body effect and by the narrow-channel effect [5]:

$$V_{T2} = V_{T2}(V_{BS2}, W_2) \tag{10}$$

We set the gate voltage V_{G2} to compensate for variations in V_{T1} and V_{T2} as follows. First, a diode-connected replica M1' of M1 is biased at the same current density so that the voltage at node A tracks the NMOS threshold ($V_{G1'} = V_{G1}$). Next, we generate the required gate-to-source voltage of the feedback device by passing a current $I_{2'}$ through diode M2'. M2' is a scaled copy of M2:

$$(W/L)_{2'} = n\,(W/L)_2 \tag{11}$$

created by laying out *n* parallel copies of M2. Since M2' has the same V_{BS} and width as M2, it experiences the same body and narrow-channel effects. Now $V_{GS2} = V_{GS2'}$ and we can write

$$V_{GS2} - V_{T2} = V_{GS2'} - V_{T2'} = \sqrt{\frac{2I_{2'}}{\mu C_{ox} n (W/L)_2}} \tag{12}$$

Substituting (12) in (6) and (7) gives for the resistance

$$R = \sqrt{\frac{n}{2I_{2'}\mu C_{ox}\left(W/L\right)_2}} \tag{13}$$

and for its sensitivity

$$\frac{dR}{R} = -\frac{1}{2}\left\{\frac{dI_{2'}}{I_{2'}} + \frac{d(\mu C_{ox})}{(\mu C_{ox})}\right\} \tag{14}$$

To first order, this resistance is independent of threshold and power supply variation. Controlling the current I_2 in the bias circuit to ±10% is straightforward, and the technological parameter (μC_{ox}) is routinely controlled in our process to ±2%.

What is more important, the resistance ***variation*** is now independent of the resistance ***value***, so we can now create a compact, high-value resistor with very low parasitic capacitance.

Our circuit uses n=500, $I_{2'}$=30μA, and $(W/L)_2$=3/20. Substitution in (10) gives a resistance of about 1.5 MΩ. Due to space constraints we implemented M2' as 50 copies of a W/L = 3/2 device instead of 500 copies of a W/L = 3/20 device. This produces a narrow-channel change in $V_{T2'}$ which increases the resistance of M2 to about 5 MΩ..

In the actual bias circuit, all currents and device widths are scaled-down to reduce the power consumption.

When detector leakage current is present, the output node (right-hand side of M2 in Fig. 2) moves positive and becomes M2's effective source. As noted in [4], this has the desirable effect of reducing the effective resistance. This fact allows us to target a higher resistance value, since on those channels with high leakage current the feedback resistance will automatically adjust itself to a lower value. Thus decreased R_F will accommodate the current without pushing the preamp output into saturation., while the noise remains dominated by the leakage current shot noise as long as the voltage drop across RF exceeds 50 mV.

From (13) we see that the resistance is proportional to $\sqrt{n / I_{2'}}$, where *n* is the number of parallel copies of the feedback device in the bias circuit and $I_{2'}$ is the drain current of M2'. The maximum resistance is dictated by the practical considerations of controlling small bias currents and layout area of large numbers of copies of M2. Assuming $I_{2'}$ > 10 nA and *n* < 2000, the achievable resistance is limited to about 10^9 Ω. It is possible to produce higher resistance values by careful adjustment of the gate voltage of the feedback transistor, but the MOS source and drain diode leakage currents limit R_{max} to about 10^{10} Ω at 300 ºK.

II.2 Nonlinear Pole-Zero Cancellation

The linearity of the non-saturated MOSFET resistor is poor for drain-source voltages more than about 50 mV. The preamplifier output may swing up to 1V in response to either a large input signal or high detector leakage current. When

this happens, the feedback MOSFET's equivalent resistance decreases. This moves the preamp feedback pole to higher frequencies. In the case of large signal charge, there will be a non-exponential decay of the preamp pulse.

We use a variation of the classical pole-zero cancellation technique [6] to accurately cancel the preamp pole including its nonlinearity. The principle is illustrated in Fig. 3. Transistor M3 is a scaled copy of feedback device M2:

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_2 \cdot \frac{C_1}{C_F} \tag{15}$$

and its gate is biased to the same potential as M2. (The input of the shaping stage is at the same DC potential as the preamp input). For low leakage current and very small signals, the two transistors behave as resistors according to (6) and the M3-C1-R1 network cancels the M2-CF pole as in the classical circuit.

Consider now the case when there is a large signal swing on the output node, or large leakage currents. Note that the gates and sources of M2 and M3 are tied together, and that their drains are both at virtual ground. Thus when the preamp output rises in response to a pulse of charge, the two transistors' bias conditions track each other exactly. That is, $V_{DS3} = V_{DS2}$, $V_{GS3}=V_{GS2}$. So the zero of the compensation network adjusts dynamically to cancel the changing pole from M2/C_F. This allows us to build a conventional shaping circuit with good overall linearity over a wide dynamic range and insensitivity to leakage current.

II.3 Shaper

The shaper stage, also shown in Fig. 3, is built around the same folded cascode amplifier used in the preamp. The bridged-T feedback network generates two poles and one zero:

$$A_v(s) = A_0 \frac{1 - s/\omega_z}{1 + s/Q\omega_0 + s^2/\omega_0^2} \tag{16}$$

where

$$\tau_z = -1/\omega_z = R_T C_3 / 2,$$

$$\tau_0 = -1/\omega_0 = R_T \sqrt{C_2 C_3},$$

and

$$Q = \sqrt{C_3 / C_2} / 2.$$

In this circuit the zero cancels the pole from the preceding pole-zero stage and the complex poles have τ_0 = 34 nsec and Q = 0.707, giving a good semiGaussian shape with a peaking time of about 50 nsec. The shaper dissipates 2.9 mW of power.

III. Experimental Details

We fabricated the IC in a 1.2 μm, double metal n-well CMOS process with an analog capacitor option. The capacitors are MOS type, with a heavily implanted bottom plate. We used polysilicon resistors except in the feedback and pole-zero cancelling circuit.

The test chip included six circuit variations to allow us to investigate the circuit blocks in detail. We included preamplifier-shapers as described in Section II, and preamplifiers without shapers but with source followers for driving an off-chip load. For each type of circuit, we included versions with and without ESD protection networks. These networks (field oxide

transistors and gate-source shorted FETS to each supply) were estimated to add 0.2 - 0.4 pF to the input capacitance. Each channel also had a 50 fF capacitor for injecting charge into the input. A microphotograph of the IC is shown in Fig. 4.

For studying the behavior of the feedback device, we brought out node DM1' (Fig. 2) to a pad. This allowed us to force the gate voltage to a level other than the natural condition established by the bias circuit.

The unpackaged die were wirebonded directly to a small FR-4 test board, which provided access to the test inputs, bias control, and output. The preamplifier inputs could be wirebonded to a small Si photodiode (capacitance about 1 pF) for studying the circuit with detector signals from radioactive sources. On this carrier we also placed a precisely measured injection capacitor for calibration and a 1MΩ chip resistor for simulating leakage current. We could select either the diode, capacitor, or resistor by wirebonding.

The circuit, with minor modifications, was also fabricated in a 2.0 μm double-metal, double-poly process.

In the next section, results refer to the 1.2 μm fabrication unless otherwise stated.

IV. Results

IV.1 MOS Feedback resistor

By measuring the decay time of the preamplifier, we get an estimate of the resistance of the MOS feedback resistor:

$$R_{eq} = \frac{t_{90-10}}{2.2 \cdot C_F} \tag{17}$$

where t_{90-10} is the 90%-10% falltime and C_F is the feedback capacitance. The measured values of the resistance for the 2.0 μm and 1.2 μm designs were 1.8 and 6.2 MΩ, respectively. The 2.0 μm design was fabricated twice in separate runs, and the mean resistance value was the same. These measured values are about 20-30% higher than the simulated ones.

We also measured the temperature dependence of the feedback resistance. Figure 5 shows the preamp's decay as the temperature is varied from -75º C to +25º C. This measurement demonstrates the effectiveness of the adaptive bias scheme. The resistance remains constant to 10% while the MOSFET threshold voltages vary by more than 200 mV over this range. Figure 6 shows the preamplifier output as the leakage current is varied from 0 to 200 nA. The change in the effective feedback resistance can be seen by the decrease in falltime and the decrease in the DC level shift as the leakage current rises.

Figure 7 shows the preamplifier output with increasing injected charge from 25 to 100 fC. Although the feedback resistance changes for high injected charge over this dynamic range, the gain is still linear to better than 1%.

By forcing the gate voltage of the feedback PMOS FET to more positive values, we could increase its effective resistance as shown in Fig. 8 (a) and (b). The useful resistance range of this device extends over 4 orders of magnitude, from 2.7×10^6 to 2.2×10^{10} Ω.

IV.2 Preamplifier Noise

We first measured the preamplifier's noise using an external, variable pulse shaper. Fig. 9 shows the equivalent input noise charge (ENC) as a function of shaping time for two bias conditions. For the self-biased condition, the series white-, 1/f-, and parallel-noise dominated regimes can be recognized by their $t_s^{-1/2}$, t_s^0, and $t_s^{1/2}$ behavior, respectively. [7]. When the feedback is biased into a higher-resistance condition, the parallel noise vanishes and we observe the noise floor due to the 1/f noise of the input NMOS transistor of about 35 e^- r.m.s. [8]. Also shown in Fig. 9 is the noise of a preamplifier with input ESD protection network. The protection network capacitance raises the series noise by about 10 e^-.

The noise vs. shaping time measurement was repeated on an ESD-protected part with feedback MOSFET pinched-off at -25 and -75 ºC. Although the series white noise showed the expected decrease (to about 58 e^- at 50 nsec), the 1/f noise floor was unchanged. This is consistent with others' measurements of a temperature-independent 1/f noise in NMOS [9].

IV.3 Integrated Preamp/Shaper

Fig. 10 shows the output waveform of the integrated preamp/shaper (lower trace) as the bias condition of the feedback (M2) and pole-zero canceling (M3) devices are varied together. The preamp output is also shown for comparison (upper trace).

Note that regardless of the decay time of the preamplifier, the shaper output waveform is practically invariant. The gain of the integrated preamp/shaper is 16.5 mV/fC. It is linear to 0.3% over a dynamic range of 50 fC, again confirming the effectiveness of the nonlinear cancellation technique.

We also studied the integrated preamp/shaper as leakage current and temperature were varied. The results are shown in Fig. 11 and Fig. 12. In Fig. 11, the gain increases about 10% for currents from 0 to 600 nA while the shape is unaffected. In Fig. 12, we see that when the temperature is reduced to -75 ºC, the shaping time decreases by 6 nsec while the gain is stable to within 3% of its room temperature value.

The noise of the integrated preamp/shaper is shown in Table 2., where we compare protected and unprotected circuits with their feedback and pole-zero canceling devices in the self-biased and pinched-off conditions.
By comparing these results with Fig. 9, we see that the integrated shaper adds 25-35 e^- noise. This is mainly due to the second stage resistor R1 (see Fig. 3), whose noise contribution is non-negligible.

IV.4 Measurements with Silicon Detector

We measured the spectra of radioactive sources with a small Si diode detector (C ~ 1 pF, I_L < 0.1 nA) wirebonded to the preamplifier. This allowed us to make an independent measurement of gain and noise.

Fig. 13 shows a spectrum of ^{241}Am taken with an ESD-protected preamplifier with M2 pinched off. An external shaper with 1 μs peaking time was used. Peaks at 7.8, 11.73, 13.94, 17.44, 20.8, 26.2, and 59.5 keV are clearly seen. From the FWHM we find a noise of 148 r.m.s. e^-. Allowing for an estimated 0.3 pF capacitance due to 2 bond wires and ~1cm PC board traces and 1.36 pF for the detector gives a noise slope of 58 e^-/pF for the preamplifier.

Fig. 14 (a) shows the spectrum of the same source taken with the integrated preamp/shaper in its self-biased condition. The noise is now 255 r.m.s. e^-. Compared to Fig. 13, there is a substantial increase in white series noise at the shorter shaping time (50 nsec) of the integrated shaper. With the feedback device pinched and at a temperature of -75 ºC, the spectrum of Fig. 14 (b) is obtained, which has 180 e^- noise.

In Fig. 15 we show the waveform of an ionizing event from a 59.5 keV photon as amplified by the integrated preamp/shaper with M2 pinched at T=+15 ºC.

V. Discussion

V.1 Noise Parameters

We analyzed the preamplifier noise data of Section IV.2 to extract the key parameters for each of the 3 noise sources. Knowledge of these parameters allows us to predict the preamplifier behavior in other conditions and guides new design efforts.

V.1.1 Series Thermal Noise

The ENC due to all white series noise sources is

$$ENC_{sw} = \sqrt{\xi\, 4kTR_s C_T^2 / \tau_m} \tag{18}$$

where R_s is the equivalent series thermal noise resistance, C_T is the total capacitance at the input, τ_m is the peaking time, and ξ is a form factor which for CR-RC2 shaping equals 0.85. From the data of Fig. 9 for 20 nsec < τ_m < 1μs we find R_s = 400 Ω. For an ideal preamplifier with g_{m1} = 3.5 mS, $R_s = 2/3g_m$ = 190Ω. Rs is increased by excess noise in the input transistor and by the secondary noise sources mentioned in Section II.

V.1.2 1/f noise

From [7] ,

$$ENC_f = \sqrt{4K_f / C_g} \cdot C_T \tag{19}$$

where K_f is the flicker noise coefficient as defined in [10]. We isolate the 1/f noise in the long-τ_m region where series thermal noise is negligible and with the feedback FET pinched off to eliminate parallel noise. From the data of Fig. 9 we find K_f = 6.9x10^{-24} J. This is close to the median value reported in the literature for NMOS [3,4,9,11].

V.1.2 Parallel Noise

In Fig. 9 this noise clearly dominates when the feedback FET is in its self-biased state and τ_m is long. We analyze this region using

$$ENC_p = \sqrt{\kappa \cdot 2kT\tau_m / R_p} \tag{20}$$

where κ=0.64 for CR-RC^2 shaping., to find R_p = 6.3MΩ.

On preamplifiers fabricated in the 2.0 μm process, we checked for consistency of effective R_F determined from falltime and parallel noise measurements. From Eq. (6), we expect $1/R_F$ to be proportional to (V_{GS}-V_T) of the feedback FET. Therefore, we plotted $1/R_F$ as the feedback FET's V_G was forced over a range of values. The results are shown in Fig. 16. The plot is a straight line when M2 is in the strong inversion region. From the slope and intercept, we can find the hole mobility and threshold voltage of the feedback device. We find μ_p=150 cm^2/V-sec and V_{T2} = -1.47 V. The noise measurements (squares) yielded R_P values that were consistent with the falltime results.

VI. Conclusions

A CMOS preamplifier and shaper circuit, capacitance-matched to detectors in the sub-1pF range, has been developed. Its key features include:

- low noise
- high linearity
- continuously sensitive
- no digital signals on chip
- no external components or critical adjustments needed

The performance of the preamp/shaper is summarized in Table 3.

A 16-channel version of the chip will be used with silicon drift detectors for particle tracking at fixed-target and collider experiments. Circuit techniques developed will be useful in designing preamplifiers for other low-capacitance detectors.

Acknowledgments

The authors wish to thank A. Kandasamy, R. Beutenmuller, and D. Pinelli for their excellent technical support, and V. Radeka for his guidance and encouragement of this project. G. Gramegna wished to thank F. Corsi, Politecnico di Bari, for his encouragement throughout this work.

References

1. E. Gatti, P. Rehak, Nucl. Instr. and Meth. 225 (1984) 608 and P. Rehak, et. al., Nucl. Instr. and Meth. A235 (1985) 224

2. STAR Collaboration, "Conceptual Design Report for the Solenoidal Tracker at RHIC (STAR)", BNL, June 15, 1992

3. Z.Y. Chang, W. Sansen, *Low Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Kluwer Academic Publishers, 1991, Ch. 5

4. E. Beuville et. al., "AMPLEX, a Low-Noise, Low-Power Analog CMOS Signal Processor for Multi-Element Silicon Particle Detectors", Nucl. Instr. Meth. A288 (1990), 157-167

5. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill 1987 191-194

6. R. A. Boie, A. T. Hrisoho, P. Rehak, "Signal Shaping and Tail Cancellation for Gas Proportional Detectors at High Counting Rates", Nucl. Instrum. Meth. 192 (1982), 365-374

7. V. Radeka, "Low Noise Techniques in Detectors", Ann. Rev. Nucl. Part. Sci. 1988. 38: 217-77

8. Sansen, W. "Limits of Low Noise Performance of Detector Readout Front Ends in CMOS Technology", IEEE Trans. Circuits and Systems 37(11), Nov. 1990, 1375-1382

9. J. Chang, A. Abidi, C. Viswanathan, "Flicker Noise in CMOS Transistors from Subthreshold to Strong Inversion at Various Temperatures", IEEE Trans. Electron Devices 41(11), Nov. 1994, 1965-1971

10. P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed., John Wiley 1984, p. 666

11. S. Tedja, H. H. Williams, J. Van der Spiegel, F. M. Newcomer, R. Van Berg, “Noise Measurement Results of a Radiation Hardened CMOS 1.2 μm P-well Process”, Nucl. Instrum. Meth. A312, 1992, 576